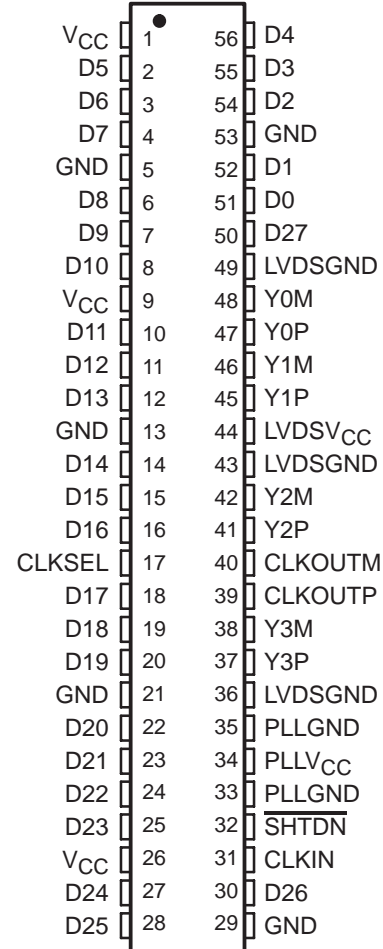- **4:28 Data Channel Compression at up to 238 MBytes/s Throughput**
- **Suited for SVGA, XGA, or SXGA Display Data Transmission From Controller to Display With Very Low EMI**
- **28 Data Channels and Clock-In Low-Voltage TTL**
- **4 Data Channels and Clock-Out Low-Voltage Differential**
- **Operates From a Single 3.3-V Supply With 250 mW (Typ)**
- **ESD Protection Exceeds 6 kV**
- **5-V Tolerant Data Inputs**
- **Selectable Rising or Falling Edge-Triggered Inputs**
- **Packaged in Thin Shrink Small-Outline Package With 20-Mil Terminal Pitch**
- **Consumes Less Than 1 mW When Disabled**
- **Wide Phase-Lock Input Frequency Range . . . 31 MHz to 68 MHz**
- **No External Components Required for PLL**
- **Outputs Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Improved Replacement for the DS90C581**

DGG PACKAGE
(TOP VIEW)

V_{CC}	1	56	D4
D5	2	55	D3
D6	3	54	D2
D7	4	53	GND
GND	5	52	D1
D8	6	51	D0
D9	7	50	D27
D10	8	49	LVDSGND
V_{CC}	9	48	Y0M
D11	10	47	Y0P
D12	11	46	Y1M
D13	12	45	Y1P
GND	13	44	LVDSV$_{CC}$
D14	14	43	LVDSGND
D15	15	42	Y2M
D16	16	41	Y2P
CLKSEL	17	40	CLKOUTM
D17	18	39	CLKOUTP
D18	19	38	Y3M
D19	20	37	Y3P
GND	21	36	LVDSGND
D20	22	35	PLLGND
D21	23	34	PLLV$_{CC}$
D22	24	33	PLLGND
D23	25	32	$\overline{\text{SHTDN}}$
V_{CC}	26	31	CLKIN
D24	27	30	D26
D25	28	29	GND

description

The SN75LVDS83 FlatLink transmitter contains four 7-bit parallel-load serial-out shift registers, a 7× clock synthesizer, and five low-voltage differential-signaling (LVDS) line drivers in a single integrated circuit. These functions allow 28 bits of single-ended low-voltage TTL (LVTTL) data to be synchronously transmitted over five balanced-pair conductors for receipt by a compatible receiver, such as the SN75LVDS82. The SN75LVDS83 can also be used in 21-bit links with the SN75LVDS86 receiver.

When transmitting, data bits D0 through D27 are each loaded into registers upon the edge of the input clock signal (CLKIN). The rising or falling edge of the clock can be selected by way of the clock select (CLKSEL) terminal. The frequency of CLKIN is multiplied seven times (7×) and then used to unload the data registers in 7-bit slices and serially. The four serial streams and a phase-locked clock (CLKOUT) are then output to LVDS output drivers. The frequency of CLKOUT is the same as the input clock, CLKIN.

The SN75LVDS83 requires no external components and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user. The only user intervention is the possible use of the shutdown/clear ($\overline{\text{SHTDN}}$) active-low input to inhibit the clock and shut off the LVDS output drivers for lower power consumption. A low-level signal on $\overline{\text{SHTDN}}$ clears all internal registers to a low level.

The SN75LVDS83 is characterized for operation over free-air temperature ranges of 0°C to 70°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FlatLink is a registered trademark of Texas Instruments.

TEXAS INSTRUMENTS

functional block diagram
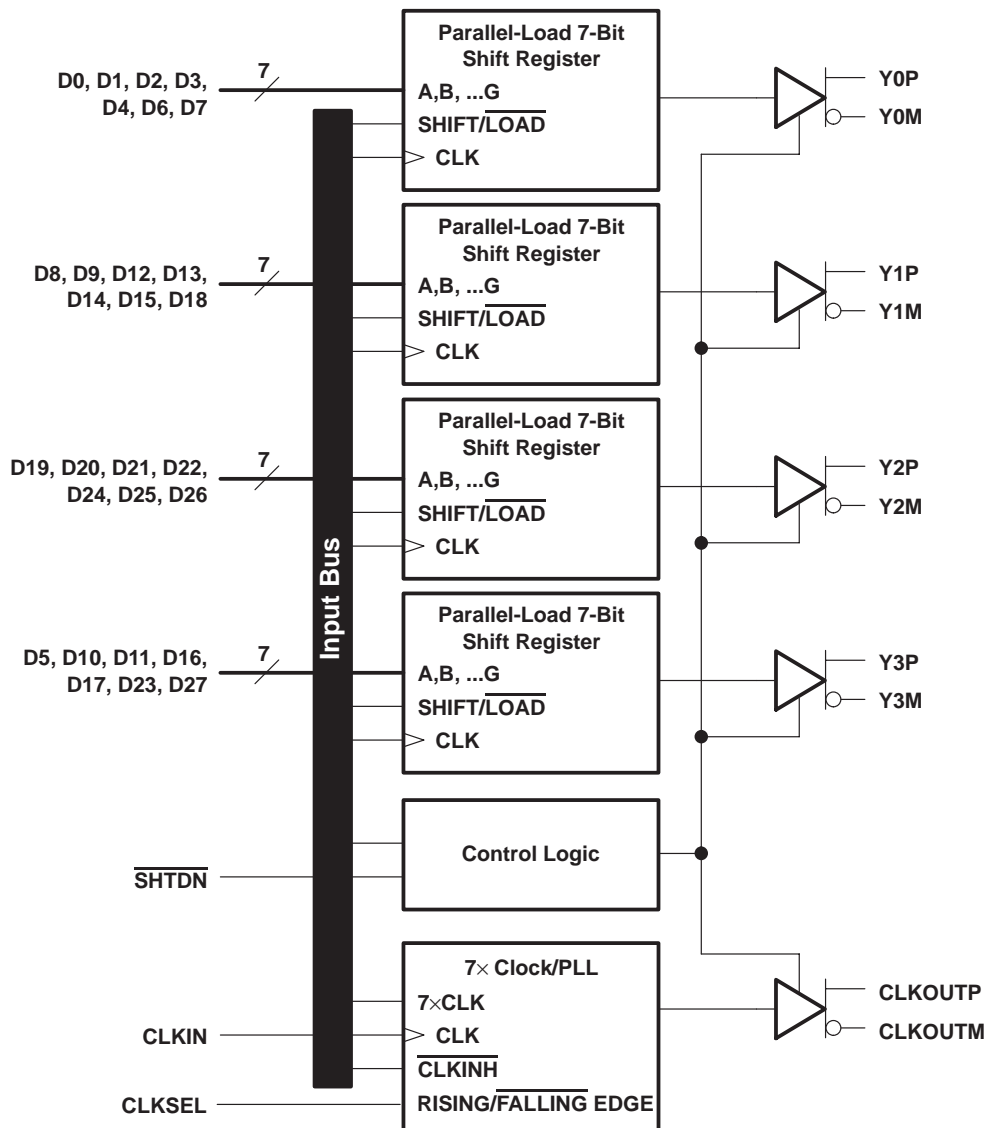
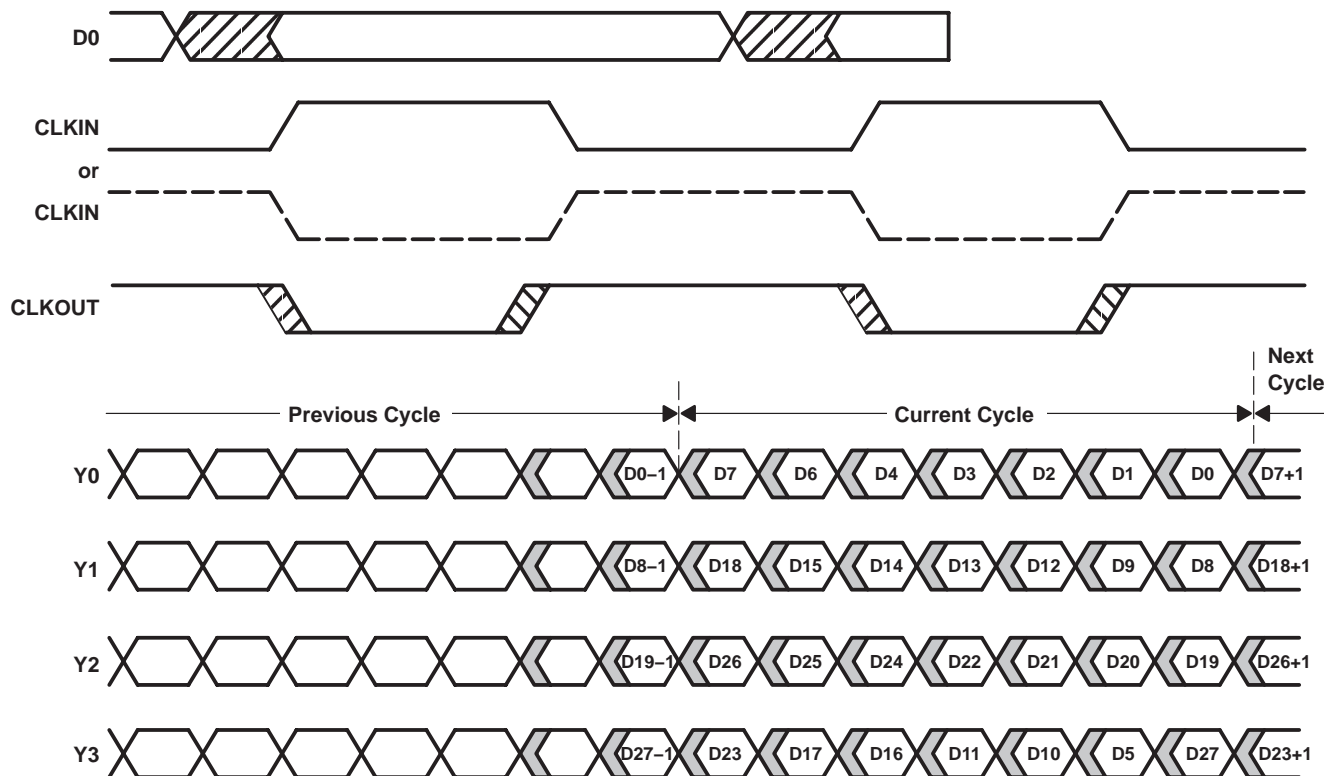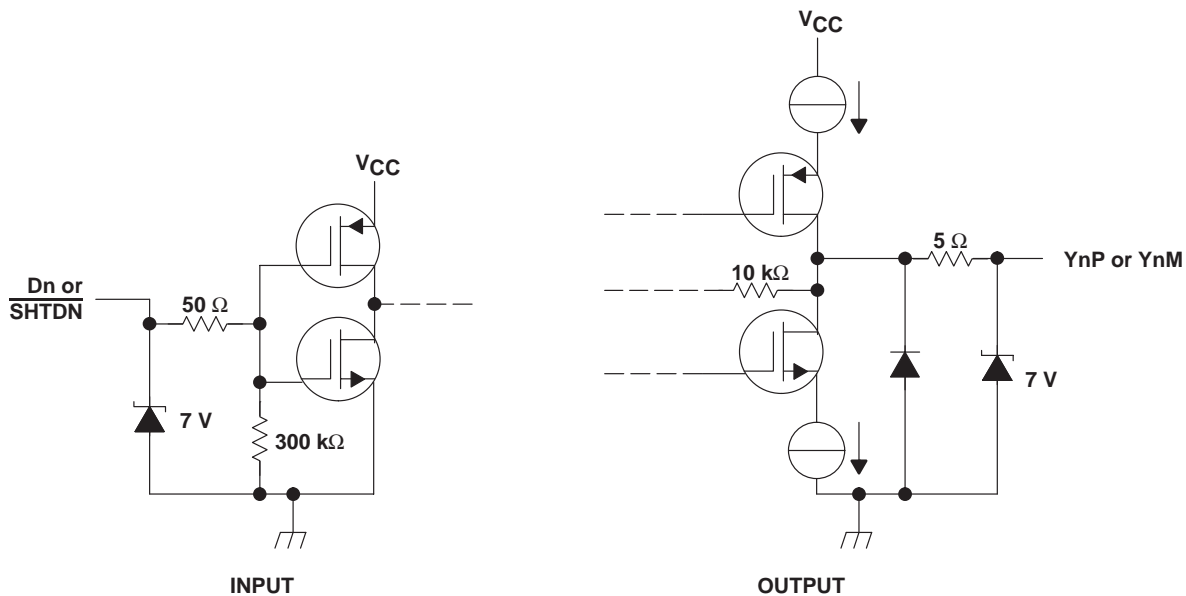Figure 1. SN75LVDS83 Load and Shift Timing Sequences

equivalent input and output schematic diagrams

SN75LVDS83
FlatLink™ TRANSMITTER

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . –0.5 V to 4 V
Output voltage range, V_O (all terminals) . . . . –0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I (all terminals) . . . . –0.5 V to 5.5 V
Continuous total power dissipation . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1:   All voltage values are with respect to the GND terminals.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING
DGG	1377 mW	11.0 mW/°C	822 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board mounted and
  with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Differential load impedance, Z_L		90		132	Ω
Operating free-air temperature, T_A		0		70	°C

timing requirements

		MIN	NOM	MAX	UNIT
t_c	Cycle time, input clock	14.7		32.3	ns
t_w	Pulse duration, high-level input clock	$0.4 t_c$		$0.6 t_c$	ns
t_t	Transition time, input signal			5	ns
t_{su}	Setup time, data, D0 – D27 valid before CLKIN↑ or CLKIN↓ (see Figure 2)	3			ns
t_h	Hold time, data, D0 – D27 valid after CLKIN↑ or CLKIN↓ (see Figure 2)	1.5			ns

electrical characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT}	Input threshold voltage			1.4		V
$|V_{OD}|$	Differential steady-state output voltage magnitude	$R_L = 100\ \Omega$, See Figure 3	247		454	mV
$\Delta|V_{OD}|$	Change in the steady-state differential output voltage magnitude between opposite binary states				50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				150	mV
I_{IH}	High-level input current	$V_{IH} = V_{CC}$			25	µA
I_{IL}	Low-level input current	$V_{IL} = 0$			±10	µA
I_{OS}	Short-circuit output current	$V_{O(Yn)} = 0$			±24	mA
		$V_{OD} = 0$			±12	mA
I_{OZ}	High-impedance state output current	$V_O = 0$ to V_{CC}			±10	µA
I_{CC}	Quiescent supply current	Disabled, All inputs at GND			280	µA
		Enabled, $R_L = 100\ \Omega$, Gray-scale pattern (see Figure 4), $V_{CC} = 3.3$ V, $t_c = 15.38$ ns		72	90	mA
		Enabled, $R_L = 100\ \Omega$, Worst-case pattern (see Figure 5), $t_c = 15.38$ ns		85	110	mA
C_I	Input capacitance			3		pF

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25°C$.

switching characteristics over recommended operating conditions (unless otherwise noted)

|	PARAMETER	TEST CONDITIONS	MIN	TYP[†]	MAX	UNIT
t_{d0}	Delay time, CLKOUT↑ to serial bit position 0		−0.2	0	0.2	ns
t_{d1}	Delay time, CLKOUT↑ to serial bit position 1		$\frac{1}{7}t_c - 0.2$		$\frac{1}{7}t_c + 0.2$	ns
t_{d2}	Delay time, CLKOUT↑ to serial bit position 2		$\frac{2}{7}t_c - 0.2$		$\frac{2}{7}t_c + 0.2$	ns
t_{d3}	Delay time, CLKOUT↑ to serial bit position 3	t_c = 15.38 ns (± 0.2%), |Input clock jitter| < 50 ps[‡], See Figure 6	$\frac{3}{7}t_c - 0.2$		$\frac{3}{7}t_c + 0.2$	ns
t_{d4}	Delay time, CLKOUT↑ to serial bit position 4		$\frac{4}{7}t_c - 0.2$		$\frac{4}{7}t_c + 0.2$	ns
t_{d5}	Delay time, CLKOUT↑ to serial bit position 5		$\frac{5}{7}t_c - 0.2$		$\frac{5}{7}t_c + 0.2$	ns
t_{d6}	Delay time, CLKOUT↑ to serial bit position 6		$\frac{6}{7}t_c - 0.2$		$\frac{6}{7}t_c + 0.2$	ns
$t_{sk(o)}$	Output skew, $t_n - \frac{n}{7}t_c$		−0.2		0.2	ns
t_{d7}	Delay time, CLKIN↓ to CLKOUT↑	t_c = 18.51 ns (± 0.2%), |Input clock jitter| < 50 ps[‡], See Figure 6	3.75	5.6	7.75	ns
$\Delta t_{c(o)}$	Cycle time, output clock jitter[§]	t_c = 15.38 ± 0.75 sin (2π500E3t) + 0.05 ns, See Figure 7		±70		ps
		t_c = 15.38 ± 0.75 sin (2π3E6t) + 0.05 ns, See Figure 7		±187		ps
t_w	Pulse duration, high-level output clock			$\frac{4}{7}t_c$		ns
t_t	Transition time, differential output (t_r or t_f)	See Figure 3	260	700	1500	ps
t_{en}	Enable time, $\overline{\text{SHTDN}}$↑ to phase lock (Yn valid)	See Figure 8		1		ms
t_{dis}	Disable time, $\overline{\text{SHTDN}}$↓ to off state (CLKOUT low)	See Figure 9		250		ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
[‡] \|Input clock jitter\| is the magnitude of the change in the input clock period.
[§] Output clock jitter is the change in the output clock period from one cycle to the next cycle observed over 15 000 cycles.
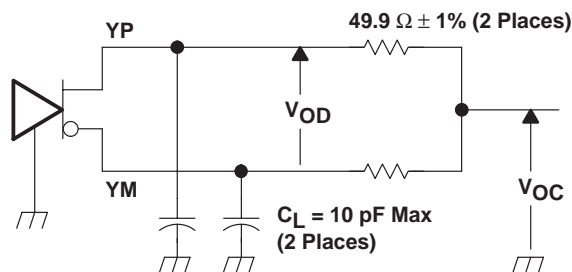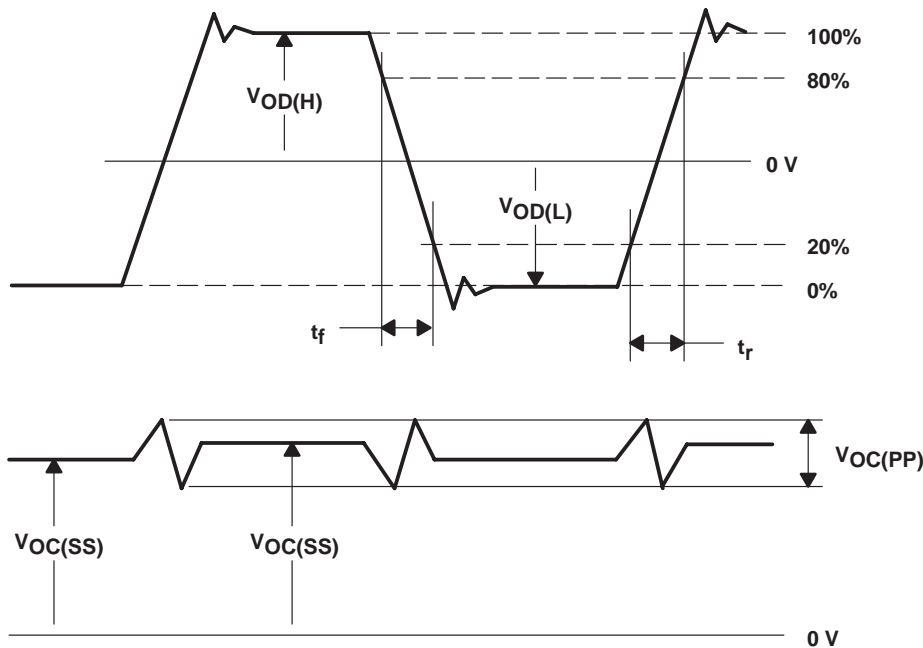
PARAMETER MEASUREMENT INFORMATION
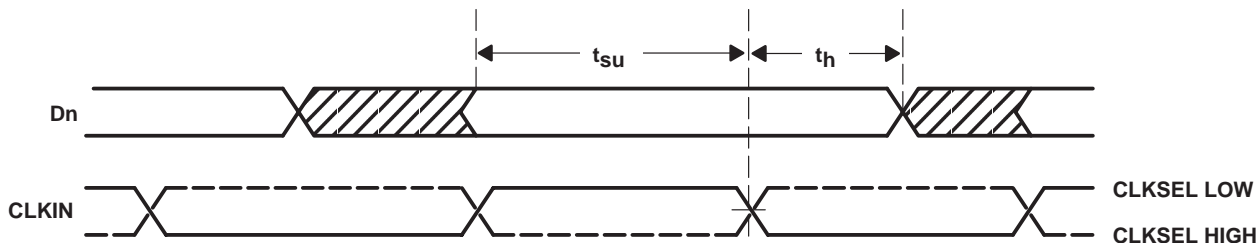
NOTE A: All input timing is defined at 1.4 V on an input signal with a 10%-to-90% rise or fall time of less than 5 ns.

Figure 2. Setup and Hold Time Waveforms

NOTE A: The lumped instrumentation capacitance for any single-ended voltage measurement is less than or equal to 10 pF. When making measurements at YP or YM, the complementary output is similarly loaded.
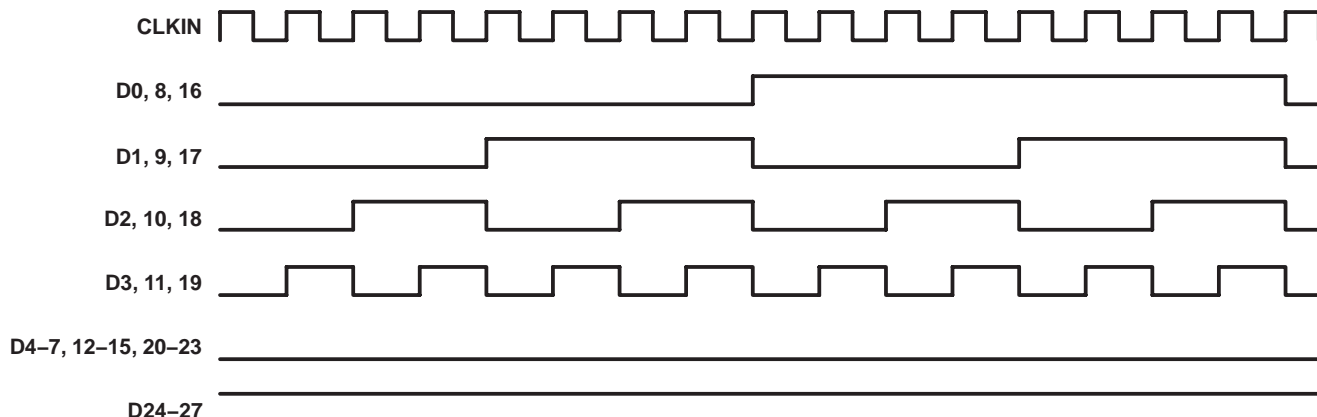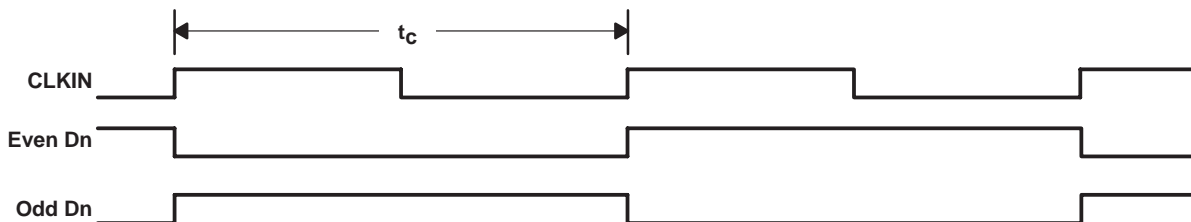
(a) SCHEMATIC

(b) WAVEFORMS

Figure 3. Test Load and Voltage Waveforms for LVDS Outputs

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

NOTE A: The 16-grayscale test-pattern test device power consumption for a typical display pattern. Pattern with CLKSEL low shown.

Figure 4. 16-Grayscale Test-Pattern Waveforms

NOTE A: The worst-case test pattern produces nearly the maximum switching frequency for all of the LVDS outputs. Pattern with CLKSEL low shown.

Figure 5. Worst-Case Test-Pattern Waveforms

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PARAMETER MEASUREMENT INFORMATION

NOTES: A. This wave form is valid when CLKSEL is low.
        B. This wave form is valid when CLKSEL is high.

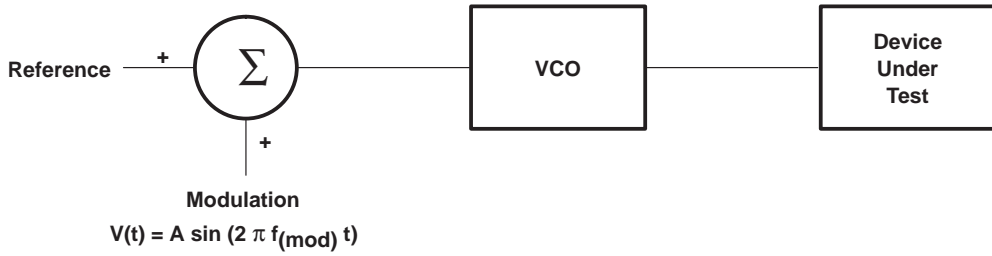**Figure 6. SN75LVDS83 Timing Waveforms**

PARAMETER MEASUREMENT INFORMATION

Reference + Σ

+ Modulation

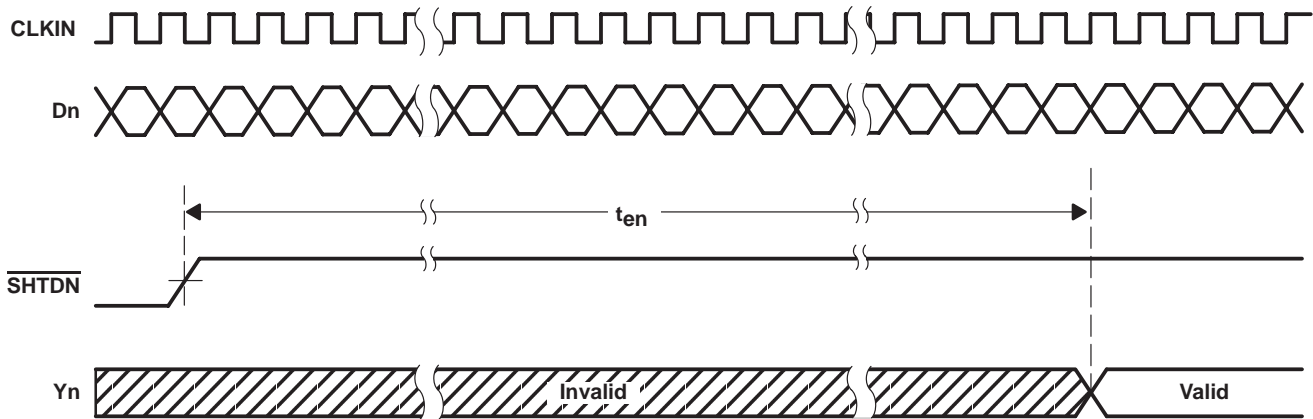$V(t) = A \sin(2 \pi f_{(mod)} t)$

VCO

Device Under Test

HP8656B Signal Generator 0.1 MHz – 990 MHz — RF Output

HP8665A Synthesized Signal Generator 0.1 MHz – 4200 MHz — OUTPUT — Modulation Input

Device Under Test — CLKIN — CLKOUT

DTS2070C Digital Time Scope — Input
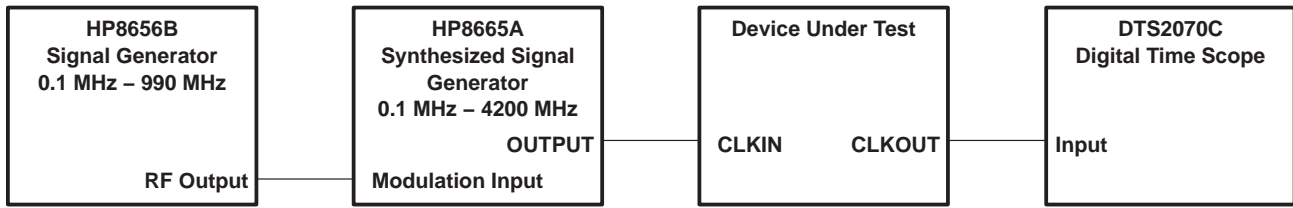
Figure 7. Output Clock Jitter Testing

CLKIN, Dn, t_{en}, SHTDN, Yn (Invalid / Valid)

Figure 8. Enable Time Waveforms

CLKIN, SHTDN, CLKOUT, t_{dis}
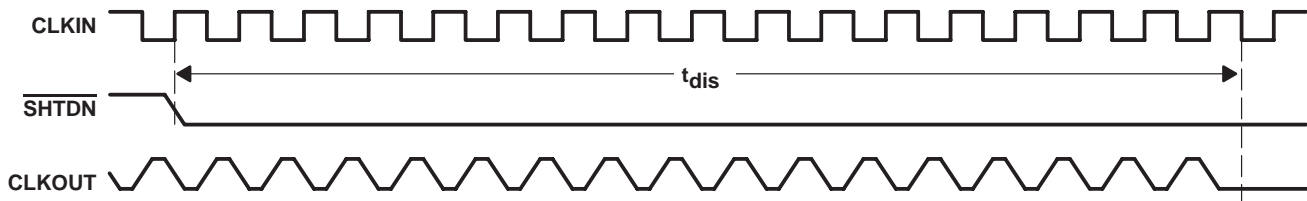
Figure 9. Disable Time Waveforms

TEXAS INSTRUMENTS

10 POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT
vs
CLOCK FREQUENCY
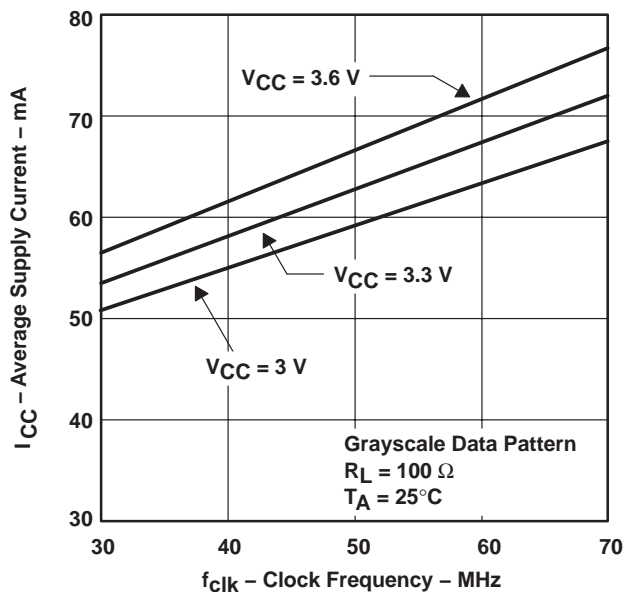
Figure 10

ZERO-TO-PEAK OUTPUT JITTER
vs
MODULATION FREQUENCY

Figure 11

SLLS271H – MARCH 1997 – REVISED JULY 2006

APPLICATION INFORMATION

Host | **Cable** | **Flat Panel Display**

Graphic Controller

12-BIT	18-BIT	24-BIT		SN75LVDS83				SN75LVDS82
RED0	RED0	RED0	51	D0	Y0M	48	9	A0M
RED1	RED1	RED1	52	D1				
RED2	RED2	RED2	54	D2	Y0P	47	10	A0P
RED3	RED3	RED3	55	D3				
RSVD	RED4	RED4	56	D4	Y1M	46	11	A1M
RSVD	RED5	RED5	3	D6				
NA	NA	RED6	50	D27	Y1P	45	12	A1P
NA	NA	RED7	2	D5				
GREEN0	GREEN0	GREEN0	4	D7				
GREEN1	GREEN1	GREEN1	6	D8	Y2M	42	15	A2M
GREEN2	GREEN2	GREEN2	7	D9				
GREEN3	GREEN3	GREEN3	11	D12	Y2P	41	16	A2P
RSVD	GREEN4	GREEN4	12	D13				
RSVD	GREEN5	GREEN5	14	D14	Y3M	38	19	A3M
NA	NA	GREEN6	8	D10				
NA	NA	GREEN7	10	D11	Y3P	37	20	A3P
BLUE0	BLUE0	BLUE0	15	D15				
BLUE1	BLUE1	BLUE1	19	D18				
BLUE2	BLUE2	BLUE2	20	D19				
BLUE3	BLUE3	BLUE3	22	D20				
RSVD	BLUE4	BLUE4	23	D21				
RSVD	BLUE5	BLUE5	24	D22				
NA	NA	BLUE6	16	D16				
NA	NA	BLUE7	18	D17				
H_SYNC	H_SYNC	H_SYNC	27	D24	CLKOUTM	40	17	CLKINM
V_SYNC	V_SYNC	V_SYNC	28	D25				
ENABLE	ENABLE	ENABLE	30	D26	CLKOUTP	39	18	CLKINP
NA	NA	RSVD	25	D23				
CLOCK	CLOCK	CLOCK	31	CLKIN				
		See Note A	17	CLKSEL				

Five 100 Ω terminating resistors shown across the differential pairs.

NOTES: A. Connect this terminal to V_{CC} for triggering to the rising edge of the input clock and to GND for the falling edge.

B. The five 100-Ω terminating resistors are recommended to be 0603 types.

Figure 12. 24-Bit Color Host To 24-Bit LCD Panel Display Application

APPLICATION INFORMATION

| Host | Cable | Flat Panel Display |

Graphic Controller

12-BIT	18-BIT	24-BIT		SN75LVDS83				SN75LVDS86
RED0	RED0	RED0	51	D0	Y0M	48	8	A0M
RED1	RED1	RED1	52	D1				
RED2	RED2	RED2	54	D2			100 Ω	
RED3	RED3	RED3	55	D3	Y0P	47	9	A0P
RSVD	RED4	RED4	56	D4				
RSVD	RED5	RED5	3	D6				
NA	NA	RED6	50	D27	Y1M	46	10	A1M
NA	NA	RED7	2	D5				
GREEN0	GREEN0	GREEN0	4	D7			100 Ω	
GREEN1	GREEN1	GREEN1	6	D8	Y1P	45	11	A1P
GREEN2	GREEN2	GREEN2	7	D9				
GREEN3	GREEN3	GREEN3	11	D12				
RSVD	GREEN4	GREEN4	12	D13	Y2M	42	14	A2M
RSVD	GREEN5	GREEN5	14	D14				
NA	NA	GREEN6	8	D10			100 Ω	
NA	NA	GREEN7	10	D11	Y2P	41	15	A2P
BLUE0	BLUE0	BLUE0	15	D15				
BLUE1	BLUE1	BLUE1	19	D18				
BLUE2	BLUE2	BLUE2	20	D19	Y3M	38		
BLUE3	BLUE3	BLUE3	22	D20				
RSVD	BLUE4	BLUE4	23	D21				
RSVD	BLUE5	BLUE5	24	D22	Y3P	37		
NA	NA	BLUE6	16	D16				
NA	NA	BLUE7	18	D17				
H_SYNC	H_SYNC	H_SYNC	27	D24				
V_SYNC	V_SYNC	V_SYNC	28	D25	CLKOUTM	40	16	CLKINM
ENABLE	ENABLE	ENABLE	30	D26				
NA	NA	RSVD	25	D23			100 Ω	
CLOCK	CLOCK	CLOCK	31	CLKIN	CLKOUTP	39	17	CLKINP
		See Note A	17	CLKSEL				

NOTES: A. Connect this terminal to V_{CC} for triggering to the rising edge of the input clock and to GND for the falling edge.
        B. The four 100-Ω terminating resistors are recommended to be 0603 types.

Figure 13. 24-Bit Color Host To 18-Bit LCD Panel Display Application

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN75LVDS83DGG	ACTIVE	TSSOP	DGG	56	35	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LVDS83DGGG4	ACTIVE	TSSOP	DGG	56	35	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LVDS83DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LVDS83DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

Reel Diameter

Reel Width (W1)

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

| Q1 | Q2 |
| Q3 | Q4 |

| Q1 | Q2 |
| Q3 | Q4 |

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVDS83DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVDS83DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0

DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
       B. This drawing is subject to change without notice.
       C. Body dimensions do not include mold protrusion not to exceed 0,15.
       D. Falls within JEDEC MO-153